

HD63B21P (XB258001) Peripheral Interface Adapter

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS}		Ground	21	R/ \overline{W}	I	Read/Write Control
2	PA ₀		Peripheral Data Bus (port A)	22	CS ₀	I	Chip Select
3	PA ₁			23	$\overline{CS_2}$	I	
4	PA ₂			24	CS ₁	I	
5	PA ₃			25	E	I	Enable
6	PA ₄			26	D ₇	I/O	Data Bus
7	PA ₅			27	D ₆	I/O	
8	PA ₆			28	D ₅	I/O	
9	PA ₇			29	D ₄	I/O	
10	PB ₀		Peripheral Data Bus (port B)	30	D ₃	I/O	
11	PB ₁			31	D ₂	I/O	
12	PB ₂			32	D ₁	I/O	
13	PB ₃			33	D ₀	I/O	
14	PB ₄			34	\overline{RES}	I	Reset
15	PB ₅			35	RS ₁	I	Register Select
16	PB ₆			36	RS ₀	I	
17	PB ₇			37	\overline{IRQB}	I	Interrupt request
18	CB ₁	I	Peripheral Control	38	\overline{IRQA}	I	
19	CB ₂	I		39	CA ₂	I	Peripheral Control
20	V _{CC}		DC Supply	40	CA ₁	I	

HA17008RP (IG154600) D/A CONVERTER

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	TC	I	Threshold Control	9	A ₅	I	Current Switch Control
2	\overline{IO}	O	Output	10	A ₆	I	
3	V _{EE}		Supply Power (–)	11	A ₇	I	
4	IO	O	Output	12	A ₈	I	
5	A ₁	I	Current Switch Control	13	V _{CC}		Supply Power (+)
6	A ₂	I		14	V _{REF +}		Reference Voltage (+)
7	A ₃	I		15	V _{REF –}		Reference Voltage (–)
8	A ₄	I		16	C	I	Compensation

HD63B50P (IG147300) Asynchronous Communications Interface Adapter

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS}		DC supply 0V	13	R/ \overline{W}	I	Read/Write
2	Rx Data	I	Receive data	14	E	I	Enable
3	Rx CLK	I	Receive clock	15	D ₇	I/O	Data bus
4	Tx CLS	O	Transmit clock	16	D ₆	I/O	
5	\overline{RTS}	I/O	Request to send	17	D ₅	I/O	
6	Tx Data	O	Transmit data	18	D ₄	I/O	
7	\overline{IRQ}	I	Interrupt request	19	D ₃	I/O	
8	CS ₀	I	Chip select	20	D ₂	I/O	
9	CS ₁	I		21	D ₁	I/O	
10	$\overline{CS_2}$	I		22	D ₀	I/O	
11	RS	I	Resist select	23	\overline{DCD}	I	Data carrier detect
12	V _{CC}		DC supply (+5.0V)	24	\overline{CTS}	I	Clear to send

HD68B09P (IG149900) CPU

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS}		Ground	21	A ₁₃	O	Address Bus
2	\overline{NMI}	I	Non-maskable Interrupt	22	A ₁₄	O	
3	\overline{IRQ}	I	Interrupt Request	23	A ₁₅	O	
4	\overline{FIRQ}	I	Fast Interrupt Request	24	D ₇	I/O	Data Bus
5	BS	O	Bus Status	25	D ₆	I/O	
6	BA	O	Bus Available	26	D ₅	I/O	
7	V _{CC}		DC supply	27	D ₄	I/O	
8	A ₀	O	Address Bus	28	D ₃	I/O	
9	A ₁	O		29	D ₂	I/O	
10	A ₂	O		30	D ₁	I/O	
11	A ₃	O		31	D ₀	I/O	
12	A ₄	O		32	R/ \overline{W}	O	Read/Write control
13	A ₅	O		33	$\overline{DMA/BREQ}$	I	DMA/Bus Request
14	A ₆	O		34	E	O	System clock
15	A ₇	O		35	Q	O	
16	A ₈	O		36	MRDY	I	Memory Ready
17	A ₉	O		37	\overline{RES}	I	Reset
18	A ₁₀	O		38	EXTAL	I	Clock
19	A ₁₁	O		39	XTAL	I	
20	A ₁₂	O		40	\overline{HALT}	I	Halt

HD63B50P (IG147300) Asynchronous Communications Interface Adapter

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS}		DC supply 0V	13	R/ \overline{W}	I	Read/Write
2	Rx Data	I	Receive data	14	E	I	Enable
3	Rx CLK	I	Receive clock	15	D ₇	I/O	Data bus
4	Tx CLS	O	Transmit clock	16	D ₆	I/O	
5	\overline{RTS}	I/O	Request to send	17	D ₅	I/O	
6	Tx Data	O	Transmit data	18	D ₄	I/O	
7	\overline{IRQ}	I	Interrupt request	19	D ₃	I/O	
8	CS ₀	I	Chip select	20	D ₂	I/O	
9	CS ₁	I		21	D ₁	I/O	
10	$\overline{CS_2}$	I		22	D ₀	I/O	
11	RS	I	Resist select	23	\overline{DCD}	I	Data carrier detect
12	V _{CC}		DC supply (+5.0V)	24	\overline{CTS}	I	Clear to send

HD68B09P (IG149900) CPU

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS}		Ground	21	A ₁₃	O	Address Bus
2	\overline{NMI}	I	Non-maskable Interrupt	22	A ₁₄	O	
3	\overline{IRQ}	I	Interrupt Request	23	A ₁₅	O	
4	\overline{FIRQ}	I	Fast Interrupt Request	24	D ₇	I/O	Data Bus
5	BS	O	Bus Status	25	D ₆	I/O	
6	BA	O	Bus Available	26	D ₅	I/O	
7	V _{CC}		DC supply	27	D ₄	I/O	
8	A ₀	O	Address Bus	28	D ₃	I/O	
9	A ₁	O		29	D ₂	I/O	
10	A ₂	O		30	D ₁	I/O	
11	A ₃	O		31	D ₀	I/O	
12	A ₄	O		32	R/ \overline{W}	O	Read/Write control
13	A ₅	O		33	$\overline{DMA/BREQ}$	I	DMA/Bus Request
14	A ₆	O		34	E	O	System clock
15	A ₇	O		35	Q	O	
16	A ₈	O		36	MRDY	I	Memory Ready
17	A ₉	O		37	\overline{RES}	I	Reset
18	A ₁₀	O		38	EXTAL	I	Clock
19	A ₁₁	O		39	XTAL	I	
20	A ₁₂	O		40	\overline{HALT}	I	Halt

MB87122 (IG153000) OPWM (Operator)

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	CDO	O	Serial data output for CD interface	40	SO	O	Serial output for waveform signal
2	CDI	I	Serial data input for CD interface	39	SI	I	Serial input for waveform signal
3	XCLK	I	Input for CD interface transmission clock	38	DT7	I	Data bus for external memory
4	$\overline{\text{CRS}}$	I	CD interface counter reset	37	DT6	I	
5	$\overline{\text{TC}}$	I	Initial clear	36	DT5	I	
6	CLK	I	3.2MHz	35	DT4	I	
7	SYW	I	Synchronization signal input	34	DT3	I	
8	MODO	I	Modulation data (vibrato)	33	DT2	I	Power supply +5V
9	MODI	I		32	DT1	I	
10	V _{SS}		Power supply ground	31	DT0	I	
11	AD0	O	Address bus for external memory	30	V _{DD}		
12	AD1	O		29	$\overline{\text{CE}}$	O	Chip enable
13	AD2	O		28	AD17	O	Address bus for external memory
14	AD3	O		27	AD16	O	
15	AD4	O		26	AD15	O	
16	AD5	O		25	AD14	O	
17	AD6	O		24	AD13	O	
18	AD7	O		23	AD12	O	
19	AD8	O		22	AD11	O	
20	AD9	O		21	AD10	O	

T7617 (IG143200) DRV3

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{DD}	I	Power supply +5V	16	SW1	I	Switch reading pin
2	SDO	O	Serial data output	15	DP1	O	LED driving pins
3	SDI	I	Serial data input	14	SW2	I	LED driving pins
4	RDO	O	Serial data output	13	DP2	O	LED driving pins
5	RDI	I	Serial data input	12	SW3	I	LED driving pins
6	ϕ	I	Clock	11	DP3	O	LED driving pins
7	G/L	I	Timing signal	10	SW4	I	LED driving pins
8	V _{SS}		Power supply ground	9	DP4	O	LED driving pins

T7648A (IG150810) DRI3

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	SDO	O	Serial data output	14	V _{DD}	I	Power supply +5V
2	SDI	I	Serial data input	13	AI	I	Rotary encoder data in (R)
3	RDO	O	Serial data output	12	BI	I	Rotary encoder data in (L)
4	RDI	I	Serial data input	11	NC		
5	ϕ	I	Clock	10	\overline{IC}	I	Initial clear
6	G/L	I	Timing for switch read, LED output.	9	$\overline{TG/L}$	O	Data output to tempo 2
7	V _{SS}	I	Power supply ground	8	NC		

T9500 (IG143300) DRVIF

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	ϕB	O	Clock output	28	V _{DD}	I	Power supply +5V
2	G/L	O	Timing signal	27	$\phi 2$	I	Clock
3	T ₂	I	Test pin	26	\overline{IC}	I	Initial clear
4	TPO	O	Data output to iG 0608	25	\overline{IRQ}	O	Interrupt output (open drain)
5	SDO	O	Serial data output	24	SDI	I	Serial data input
6	RDO	O	Serial data output	23	RDI	I	Serial data input
7	A ₀	I	Address bus	22	4/8	I	Select DRV3 or TC401
8	A ₁	I		21	TI	I	Test pin
9	A ₂	I		20	\overline{CS}	I	Chip select
10	R/W	I	Read write select	19	D ₇	I.O	Data bus
11	D ₀	I.O	Data bus	18	D ₆	I.O	
12	D ₁	I.O		17	D ₅	I.O	
13	D ₂	I.O		16	D ₄	I.O	
14	V _{SS}	I	Power supply ground	15	D ₃	I.O	

YM2403 (XA801001) OPLP (Operator)

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS1}			24	EMIH	I	Expansion input
2	V _{DD}		Power supply +5V	23	EMIL	I	
3	EMOL	O	Expansion output	22	OP OUT	O	Serial output (audio)
4	EMOH	O		21	OP IN	I	Serial input (audio)
5	PMDL	I	Pitch information input from MOD	20	AMODH	I	Amplitude data input from MOD
6	PMDH	I		19	AMODL	I	
7	XCLK	I	CD transmission clock	18	TEGH	I	Touch EG input from MOD
8	CDO	O	CD output	17	TEGL	I	
9	CDI	I	CD input	16	CLK	I	3.2MHz
10	CRS	I	CD counter reset	15	V _{SS2}		Power supply ground
11	TS	I	Test pin (V _{DD})	14	SYW	I	Synchronization signal determine starting point of DAC cycle.
12	TEST	I		13	IC	I	Initial clear

YM2404 (XA806001) OPLM (Operator)

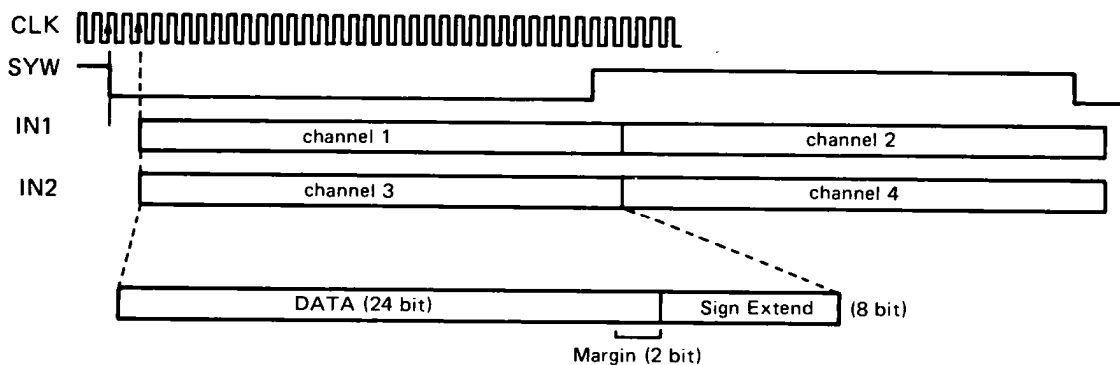
Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS}		Power supply ground	24	TESTS	I	Test pin (V _{DD})
2	CLK	I	3.2MHz	23	TESTM	I	
3	SYW	I	Synchronization signal to determine starting point of DAC cycle.	22	CDO	O	CD output
4	TEST3	I	Test pin (V _{DD})	21	CDI	I	CD input
5	TEST2	I		20	CRS	I	CD counter reset
6	TEST1	I		19	XCLK	I	CD transmission clock
7	PMDDH	I	Pitch data from MOD	18	OPOUT1	O	Serial data output (audio)
8	PMDDL	I		17	OPOUT2	O	
9	AMDDH	I	Amplitude data from MOD	16	OPIN1	I	Serial data input (audio)
10	AMDDL	I		15	OPIN2	I	
11	TEGL	I	Touch EG data from MOD	14	IC	I	Initial clear
12	TEGH	I		13	V _{DD}		Power supply +5V

YM2415 (XB641001) OPAW (Operator A type)

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	SI4	I	Serial input for waveform after envelope multiplication	64	SI3	I	Serial input for 800KHz sampling waveform data
2	MI1	I		63	SI2	I	
3	MI0	I		62	SI1	I	
4	AUXIN0	I	Extra memory data (used only for linear PCM)	61	SI0	I	Power supply +5V
5	AUXIN1	I		60	VDD		
6	AUXIN2	I		59	XCLK	I	
7	AUXIN3	I	Address bus	58	\overline{IC}	I	Initial clear
8	A20	O		57	CDI	I	Control data input
9	A19	O		56	CDO	O	Control data output
10	A18	O	Power supply ground	55	XMD	I	Control data transmission mode select
11	A17	O		54	\overline{CRS}	I	CD counter reset
12	A16	O		53	SO4	O	4 bit serial input for 800KHz sampling waveform data
13	A15	O	Address bus	52	SO3	O	
14	VSS			51	SO2	O	
15	A14	O	Address bus	50	SO1	O	SOUTO/PSYNC select
16	A13	O		49	SO0	O	
17	A12	O		48	OMD	I	
18	A11	O	Address bus	47	MO1	O	Serial output for waveform after envelope multiplication
19	A10	O		46	MO0	O	
20	A9	O		45	PMODH	I	Vibrato data from MOD
21	A8	O	Address bus	44	PMODL	I	
22	A7	O		43	TEGH	I	
23	A6	O	Address bus	42	TEGL	I	Touch data from MOD
24	A5	O		41	TST	I	
25	A4	O		40	CLK	I	
26	A3	O	Address bus	39	SYW	I	Sync signal
27	A2	O		38	D7	I	Data bus
28	A1	O		37	D6	I	
29	A0	O	Data bus	36	D5	I	
30	D0	I		35	D4	I	Power supply ground
31	D1	I		34	D3	I	
32	D2	I		33	VSS		

YM3017 (XA800001) DAC-Logic

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	DVdd		Digital power supply terminal	24	\overline{IC}	I	Initial clear
2	SYW	I	System synchronization signal input (input 31-62Y64 timing signal)	23	SEL2		Shifts up the meaningful place of the input data according to the SEL setting.
3	DGND		Digital ground terminal	22	SEL1		
4	CLK	I	Master clock input terminal, 3.2MHz.	21	IN2	I	Data input terminal. See below.
5	\overline{CRASH}	O	Indicates abnormal amplitude of input data. (Evaluates as abnormal if 23th bit and 24th bit are different.)	20	IN1	I	
6	ZERO	O	Goes high when data of all channels has been zero for 80-120mS. Open drain.	19	LMT-EN	I	Input terminal to enable limiter. 'H' enables.
7	OUT4	O	Corresponds to channels 1-4 of the analog output terminals. The DAL takes 17 bits as meaningful data, converts this into parallel data with a 10 bit mantissa and 3 bit exponent, and D/A converts this.	18	AVdd		Analog power supply terminal
8	OUT3	O		17	AGND		Analog ground terminal
9	OUT2	O		16	RB	O	The internally generated high-precision VDD/2 voltage is output, and added to the MP through the buffer op amp. The MP voltage is output through the resistance.
10	OUT1	O		15	RC	O	Used as feedback for the MP.
11	NS	I	Input terminal for chip test. Normally fixed at low.	14	MP	I	Terminal to specify center point voltage for DAC output. Normally biased at VDD/2.
12	COM	O	Output terminal for external amp	13	TO-BUF	I	Input terminal to external amp.



YM2406 (XA804001) Digital Filter

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS}		Power supply ground	24	CDI	I	CD input
2	$\overline{\text{TST}}$	I	Test pin	23	$\overline{\text{CRS}}$	I	CD counter reset
3	$\overline{\text{IC}}$	I	Initial clear	22	CDO	O	CD output
4	SI	I	32 bit x 2 channel serial	21	NC		
5	XCLK	I	CD transmission clock	20	NC		
6	SYW	I	Synchronization signal	19	NC		
7	SO	O	32 bit x 2 channel serial	18	NC		
8	CLK	I	3.2MHz	17	NC		
9	V _{DD}		Power supply +5V	16	NC		
10	NC			15	NC		
11	NC			14	NC		
12	NC			13	NC		

YM3602 (XA802001) OPRW (Operator)

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{DD}	I	Power supply +5V	40	SYW	I	31-62Y64
2	CDO	O	Cascade output pin for serial control data	39	$\overline{\text{CS}}$	O	Chip select
3	CDI	I	CD data input terminal	38	CLK	I	Master clock 3.2MHz
4	$\overline{\text{CRS}}$	I	CD counter reset	37	XCLK	I	Control data transmit clock
5	XMD	I	When CDI and XCLK are asynchronous, this is 'H'	36	$\overline{\text{IC}}$	I	Initial clear
6	D7	I	Data bus for external memory	35	A18	O	Address bus for external memory
7	D6	I		34	A17	O	
8	D5	I		33	A16	O	
9	D4	I		32	A15	O	
10	D3	I		31	A14	O	
11	D2	I		30	A13	O	
12	D1	I		29	A12	O	
13	D0	I		28	A11	O	
14	SOUT	O	Serial signal output	27	A10	O	
15	SRIN	I	Serial signal input	26	A9	O	
16	A0	O	Address bus for external memory	25	A8	O	
17	A1	O		24	A7	O	
18	A2	O		23	A6	O	
19	A3	O		22	A5	O	
20	V _{SS}	I	Power supply ground	21	A4	O	

YM3604 (XA803001) OPBW (Operator)

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{DD}		Power supply +5V	40	TST1	I	Test pin (V _{DD})
2	TST2	I	Test signal	39	A14	I	
3	SYNT	I/O	Synthesis mode	38	A13	I	
4	H/L	O	High byte/Low byte select	37	A12	I	
5	R/W	O	Read write output	36	A11	I	Address bus
6	AOE	O	Output enable	35	A10	I	
7	SO	O	Serial signal input (audio)	34	A9	I	
8	SI	I	Serial signal input (audio)	33	A8	I	
9	D0	I/O	Data bus	32	A7	I	
10	D1	I/O		31	A6	I	
11	D2	I/O		30	A5	I	
12	D3	I/O		29	A4	I	
13	D4	I/O		28	A3	I	
14	D5	I/O		27	A2	I	
15	D6	I/O		26	A1	I	
16	D7	I/O		25	A0	I	
17	CDO	O	CD data output terminal	24	CLK	I	3.2MHz
18	CDI	I	CD data input terminal	23	XCLK	I	CD transmission clock
19	CRS	I	CD counter reset	22	TC	I	Initial clear
20	V _{SS}		Power supply ground	21	SYW	I	

YM3807 (XA902001) Modulation Signal Generator

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	NC		Inputs data to add to the waveform data inside MOD	24	VSS		Power supply ground
2	MDSIO	I		23	CDO	O	CD interface serial data output
3	MDSI1	I		22	CDI	I	CD interface serial data input
4	MDSO0	O		21	NC		
5	MDSO1	O	Outputs MOD internal waveform data with the same data format as MDSIO.	20	XCLK	I	CD interface transmission clock input
6	MD0	O	Outputs waveform data for all channels inside MOD.	19	XMD	I	Selects 1/16 mode (asynchronous) or 1/1 mode (synchronous) for the CD interface
7	MD1	O		18	CRS	I	CD counter reset
8	MD2	O		17	CLK	I	3.2MHz
9	MD3	O		16	TC	I	Initial clear
10	MD4	O		15	SYW	I	Sync signal input. One 64th of the master clock.
11	MD5	O		14	MD7	O	Outputs waveform data for all channels inside MOD.
12	VDD		Power supply +5V	13	MD6	O	

YM3804 (IT380401) Digital Signal Processor

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	D15	I.O	Data bus	64	VSS		Ground
2	D14	I.O		63	D16	I.O	Data bus
3	D13	I.O		62	D17	I.O	
4	D12	I.O		61	D18	I.O	
5	D11	I.O		60	D19	I.O	
6	D10	I.O		59	D20	I.O	
7	D9	I.O		58	D21	I.O	
8	D8	I.O		57	D22	I.O	
9	D7	I.O		56	D23	I.O	
10	D6	I.O		55	MOD0	I	MOD data input terminal
11	D5	I.O		54	MOD1	I	
12	D4	I.O		53	MOD2	I	
13	D3	I.O		52	MOD3	I	
14	D2	I.O		51	MOD4	I	
15	D1	I.O		50	MOD5	I	
16	D0	I.O		49	MOD6	I	
17	ST1	I	Serial data input terminal	48	MOD7	I	Initial clear
18	ST0	I		47	\overline{IC}	I	
19	SO1	O	Serial data output terminal	46	CE	I	Chip enable
20	SO0	O		45	CLK	I	Master clock input terminal
21	XMD	I	Select internal ACIA synchroni- zation mode	44	SYW	I	Input for generating SYNC signals internally
22	XCLK	I	Time-out output terminal	43	\overline{TSTI}	I	Terminal for internal test. To enter test mode, connect to GND. When in use, VDD.
23	\overline{TO}	O	Time-out output terminal	42	\overline{TSTR}	I	
24	\overline{CRS}	I	CD counter reset	41	A0	O	Address bus
25	CDO	O	CD data output terminal	40	A1	O	
26	CDI	I	CD data input terminal	39	A2	O	
27	TIMI	O	Unconditionally outputs the 15th bit of the Address Shift Register	38	A3	O	
28	\overline{REF}	O	Three-state. Memory which needs refreshing.	37	A4	O	
29	OE	O	Three-state. Connect to memory OE.	36	A5	O	
30	R/W	O	Three-state. Memory read/write signal.	35	A6	O	
31	CAS	O	Three-state. DRAM control signal	34	A7	O	Power supply 5V
32	RAS	O		33	VDD		

YM3808 (XA798001) Digital Mixer

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{DD}		Power supply +5V	24	CLK	I	3.2MHz
2	MXI ₁	I	Input from tone generators	23	XCLK	I	500K-3.2MHz CD reception
3	MXI ₂	I		22	SYW	I	Synchronization signal to determine starting point of DAC cycle.
4	MXI ₃	I		21	MXC ₁	I	Cascade input
5	MXI ₄	I		20	MXC ₂	I	
6	MXI ₅	I		19	NC		
7	MXI ₆	I		18	$\overline{\text{TST}}$	I	Test pin (V _{DD})
8	MXI ₇	I		17	MXO1	O	Output
9	MXI ₈	I		16	MXO2	O	
10	CDI	I	CD input	15	NC		
11	$\overline{\text{CRS}}$	I	CD counter reset	14	NC		
12	V _{SS}			13	CDO	O	CD output

YM3809 (XA796001) Re Sample Filter

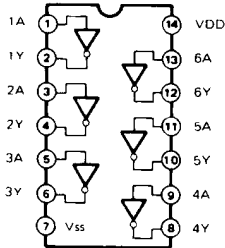
Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{SS}		GND	16	CLK	I	3.2MHz
2	IN ₀	I	Signal from OPAW	15	SYW	I	31-62Y64
3	IN ₁	I		14	(NC)		
4	IN ₂	I		13	SI	I	Serial (audio) signal input
5	IN ₃	I		12	$\overline{\text{IC}}$	I	Initial clear
6	IN ₄	I		11	(NC)		
7	SO	O	Serial (audio) signal output	10	V _{DD}	I	Power supply
8	V _{DD}	I	Power supply	9	(NC)		

YM3813 (XA799001) Micom Peripheral Hardware

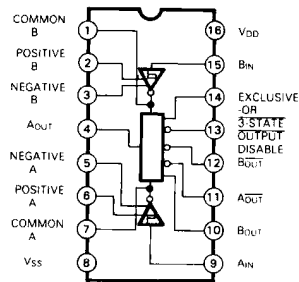
Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	$\overline{\text{ROMP}}$	O	When address for the microcomputer program ROM is 8000-FFFFh, this is low.	64	TST	I	Test pin
2	$\overline{\text{RDMD}}$	O	This is the NAND of the E, Q and OR outputs with the decoded result of address 4000-7FFFh. Low when address is 2000-3FFFh.	63	VSS	I	Power supply ground
3	$\overline{\text{SRAM}}$	O	For static RAM used in the micro-computer.	62	BANK2	O	Sends codes 0-7 for program.
4	$\overline{\text{PSRAM}}$	O	This is the NAND of the E, Q and OR outputs with the decoded result of address 0000-1BFFFh. Low when address is 1C00-1DFFFh.	61	BANK1	O	
5	$\overline{\text{PCS}}$	O	Area for other peripheral LSIs connected to the microcomputer bus.	60	BANK0	O	
6	MRDY	O	Connect to 68B09 MRDY.	59	KI	O	Resets each KBS. The same signal resets the MPH internal KDREC and EGSIM.
7	Q	I	Connect to 68B09 Q.	58	CRS	O	Counter reset for CD.
8	E	I	Connect to 68B09 E.	57	IC	O	Initializes each LSI. The same signal resets the two timers and SYW transmitter inside the MPH.
9	R/W	I	Connect to 68B09 R/W.	56	RES	I	Connect signal to be input to the micro-computer reset pin.
10	A15	I	Address bus	55	CLK	I	3.2MHz master clock.
11	A14	I		54	CDO0	O	The CD input pin data changes at the rise of XCLK. Output pin select is done by program. Simultaneous transmission is possible from multiple pins. Each CDO can be connected to 16 LSIs, each MPH can be connected to 64 LSIs.
12	A13	I		53	CDO1	O	
13	A12	I		52	CDO2	O	
14	A11	I		51	CDO3	O	
15	A10	I		50	XCLK	I	Input 500K-3.2MHz CD transmission clock.
16	A9	I	If IRQs originating outside of the MPH are to be encoded together with IRQs from inside the MPH, connect here.	49	D7	I.O	Data bus
17	A3	I		48	D6	I.O	
18	A2	I		47	D5	I.O	
19	A1	I		46	D4	I.O	
20	A0	I		45	D3	I.O	
21	$\overline{\text{RQA}}$	I		44	D2	I.O	
22	$\overline{\text{RQ9}}$	I		43	D1	I.O	
23	$\overline{\text{RQ8}}$	I		42	D0	I.O	
24	$\overline{\text{RQ7}}$	I		41	RXC	I	100K-500KHz KBS data reception clock.
25	$\overline{\text{RQ1}}$	I	Open drain output. Connect to 69B09 IRQ.	40	KDU	I	Input terminal from each KBS. Data is sampled at the rise of RXC.
26	$\overline{\text{RQ0}}$	I		39	KDL	I	
27	$\overline{\text{IRQ}}$	O		38	KDP	I	
28	$\overline{\text{TRQ}}$	O		37	KDS	I	
29	SYW	O	SYW signal output. Each LSI uses this as 32-62Y64.	36	KDX	I	Connect to each KBS. Control signal for data transmission.
30	$\overline{\text{DRX}}$	O	Connect to each LSI to control data transmission.	35	$\overline{\text{DRU}}$	O	
31	$\overline{\text{DRS}}$	O	Connect to each LSI to control data transmission.	34	$\overline{\text{DRL}}$	O	
32	VDD	I	Power supply +5V	33	$\overline{\text{DRP}}$	O	

■ IC BLOCK DIAGRAM

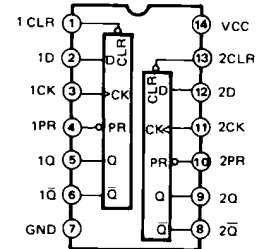
- TC74HC04P (IR000400)
- TC40H004P (IG051000)
- TC4069UBP (IG001720)
Hex Inverter



- TC4583BP (XB180001)
Dual Schmitt Trigger

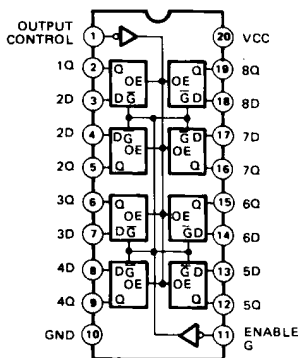


- TC40H074P (IG051100)
Dual D-Type Flip-Flop

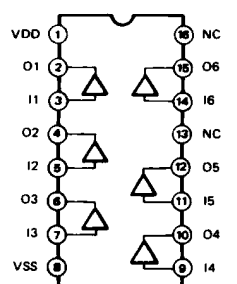


INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	?	H	H	L
H	H	?	L	L	H
H	H	L	X	Q ₀	Q ₀ -bar

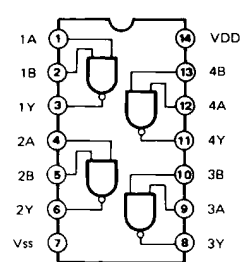
- TC40H373PYH (IG078500)
Octal 3-State D-Type Latch



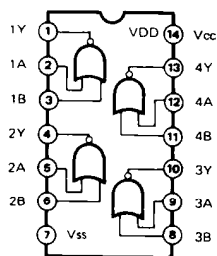
- TC50H001P (IG140900)
Hex Buffer/Converter



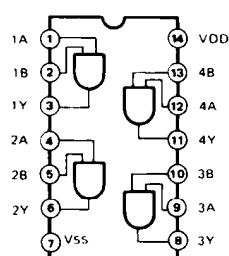
- TC74HC00P (IR000000)
Quad 2 Input NAND



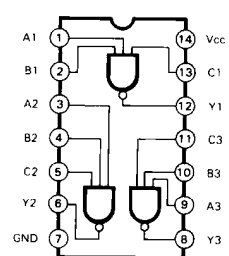
- TC74HC02P (IR000200)
Quad 2 Input NOR



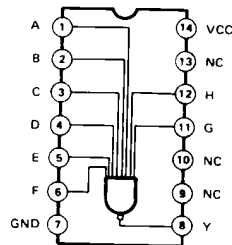
- TC74HC08P (IR000800)
Quad 2 Input AND



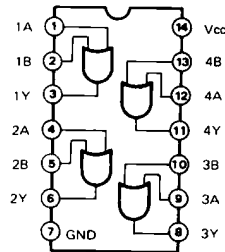
- TC74HC10P (IR001000)
Triple 3 Input NAND



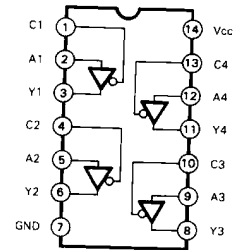
- **TC74HC30P (IR003000)**
8 Input NAND



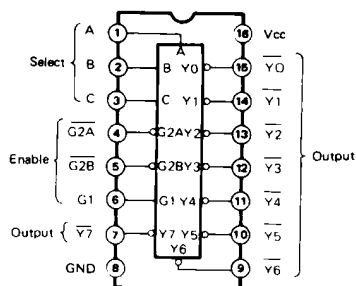
- **TC74HC32P (IR003200)**
Quad 2 Input OR



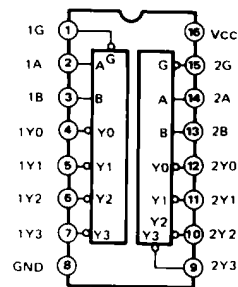
- **TC74HC125P (IR012500)**
Quad 3-State Bus Buffer



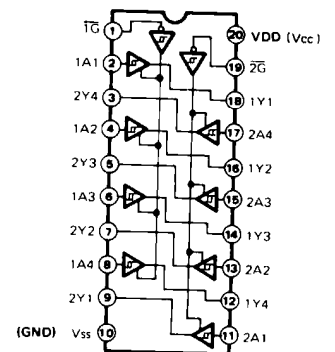
- **TC74HC138P (IR013800)**
3 to 8 Demultiplexer



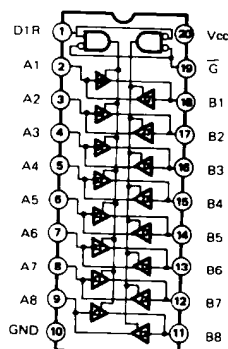
- **TC74HC139P (IR013900)**
Dual 2 to 4 Demultiplexer



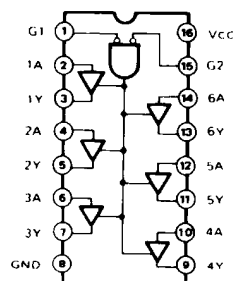
- **TC74HCT244P (XB179001)**
- **TC74HC244P (IR024400)**
Octal 3-State Bus Buffer



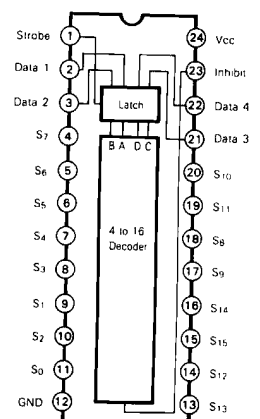
- **TC74HC245P (IR024500)**
Octal 3-State Bus Transceiver



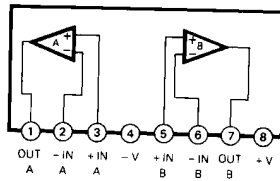
- **TC74HC365P (IR036500)**
Hex 3-State Bus Buffer



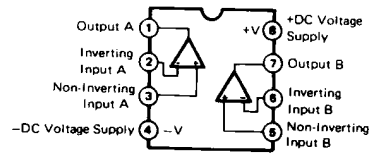
- **TC74HC4515P (IR451500)**
4-bit Latch/4 to 16-line Decoder



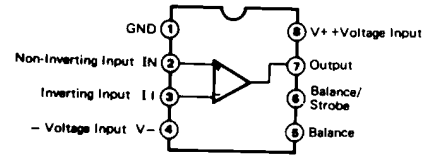
- **M5216L (XB419001)**
Dual Operational Amplifier



- **NJM4556 (IG042500)**
- **NJM4558 (IG001390)**
- **NJM4560ED (IG040000)**
Dual Operational Amplifier



- **T6400 (S) (IG079500)**
Clock Buffer



HX-3

HX-1

HX-5

MKX-5

MKX-4

KA-30

STX-1

KA-40

KA-20

KA-10

EP-20

EP-10

PKX-M1

PKX-S1

PKX-F1

BNX-M1

BNX-F1

